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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/071,106	02/08/2002	Robert L. Wood	9134-59	1445

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EXAMINER
MARTINEZ, JOSEPH P

ART UNIT	PAPER NUMBER
2873	

DATE MAILED: 01/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/071,106	WOOD, ROBERT L.	
	Examiner	Art Unit	
	Joseph Martinez	2873	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being fully anticipated by Little (5,663,596).

Re claim 1, Little teaches for example, a microelectromechanical (MEM) module comprising: a plurality of MEM device substrates, each of which includes at least one MEM device thereon; a base substrate including a face; and a mounting structure that is configured to mount the plurality of MEM device substrates on the face (col. 6, ln. 4-24). The office interprets the teachings of Little that disclose MEMs manufactured separately and consequently placed on a single substrate to teach the imitations set forth.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Little in view of Krusius et al. (6,005,649).

Re claim 2, supra claim 1. But Little fails to teach each of the MEM device substrates includes an array of M rows and N columns of MEM devices thereon and wherein the mounting structure is configured to mount the plurality of MEM device substrates in an array of R rows and S columns on the face to thereby provide a tiled array of M x R rows and N x S columns of the MEM devices in the MEM module. However, Krusius et al. teach for example, each of the MEM device substrates includes an array of M rows and N columns of MEM devices thereon and wherein the mounting structure is configured to mount the plurality of MEM device substrates in an array of R rows and S columns on the face to thereby provide a tiled array of M x R rows and N x S columns of the MEM devices in the MEM module (col. 4, ln. 43-67, col. 5, ln. 1-17). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Little and Krusius et al. to provide a compact, lightweight and inexpensive modules.

Re claim 3, supra claim 2. Krusius et al. further teach for example, the MEM devices comprise movable MEM mirrors (col. 6, ln. 21-28). The office interprets micromirror microdisplays to include movable MEM mirrors. Therefore, Krusius et al. teach the limitations set forth.

Re claim 4, supra claim 2. Little further teaches for example, the mounting structure comprises a plurality of solder bumps (solder bumps 114, fig. 6 col. 5, ln. 35-42) that are configured to mount the plurality of MEM device substrates on the face.

Re claim 5, supra claim 4. Krusius et al. further teach for example, the MEM device substrate includes first and second opposing faces, wherein the at least one MEM device is adjacent the first face and remote from the second face (fig. 6, col. 6, ln. 38-67) and wherein the

first faces of the MEM device substrates are adjacent the face of the base substrate (fig. 6, col. 6, ln. 38-67).

Claims 6-8 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krusius et al. in view of Minamoto (6,108,118) in further view of Bhalla et al. (6,275,326).

Re claim 6, Krusius et al. teach for example a microelectromechanical (MEM) mirror module comprising: a plurality of MEM mirror substrates, but fail to teach a mirror comprising monocrystalline silicon, a frame comprising monocrystalline silicon that is spaced apart from and at least partially surrounds the mirror and at least two hinges between the mirror and the frame; a base substrate including a face; and a mounting structure that is configured to mount the frames of the plurality of MEM device substrates on the face. However, Minamoto teaches for example, a mirror (mirror surface 106, fig. 2A, col. 5, ln. 7-29) comprising monocrystalline silicon (col. 5, ln. 30-55), a frame comprising monocrystalline silicon that is spaced apart from and at least partially surrounds the mirror (col. 5, ln. 30-55) and a hinge (elastic member 152, fig. 2A, col. 7, ln. 1-20) between the mirror and the frame; a base substrate including a face (movable plate 101, fig. 2A, col. 5, ln. 7-29); and a mounting structure (support 103, fig. 2A, col. 5, ln. 7-29) that is configured to mount the frames of the plurality of MEM device substrates on the face, but fail to teach at least two hinges between the mirror and the frame. However, Bhalla et al. teach for example, at least two hinges (springs 19, fig. 1, col. 2, ln. 54-67, col. 3, ln. 1-7) between the mirror and the frame. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Krusius et al., Minamoto and Bhalla et al. in order to provide an array of movable mirrors made of silicon for stiffness with a plurality of hinges for movability.

Re claim 7, supra claim 6. Minamoto further teaches for example, the frame is a first frame (movable plate 101, fig. 5A, col. 7, ln. 49-67, col. 8, ln. 1-11), each of the MEM mirror substrates also comprising an insulator layer (insulating film 102, fig. 5A, col. 7, ln. 49-67, col. 8, ln. 1-11) on the first frame, opposite the mounting structure, and a second frame that is thicker than the first frame (permanent magnet 108, the Hall element 108, and the Hall element wiring 109 are formed integral with one another in a monolithic form, col. 5, ln. 7-29) on the insulator layer opposite the first frame (fig. 5A, col. 7, ln. 49-67, col. 8, ln. 1-11). The office interprets the monolithic formation taught by Minamoto (fig. 2B) to be a layer on the insulating layer opposite the movable plate and therefore teaches the limitations set forth.

Re claim 8, supra claim 6. Minamoto further teaches for example, the mirror includes a pair of opposing faces and wherein each of the MEM mirror substrates further comprises a metal layer on each of the opposing faces of the mirrors (col. 5, ln. 42-45, col. 8, ln. 5-10).

Re claim 11, Minamoto further teaches for example, the MEM mirror substrates includes an array of M rows and N columns of MEM mirrors thereon and wherein the mounting structure is configured to mount the plurality of MEM mirror substrates in an array of R rows and S columns on the face to thereby provide a tiled array of M x R rows and N x S columns of the MEM mirrors in the MEM mirror module (col. 4, ln. 53-58).

Claims 12-15 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krusius et al. in view of Minamoto.

Re claim 12, Krusius et al. teach for example, a MEM module, but fail to teach a method of fabricating comprising: providing a silicon-on-insulator substrate that includes a monocrystalline silicon layer on a bulk silicon substrate, with an insulator layer therebetween;

fabricating at least two spaced apart pads in the monocrystalline silicon layer that extend through the monocrystalline silicon layer to the insulator layer; fabricating at least one hinge on each of the at least two spaced apart pads; defining a mirror and a frame that at least partially surrounds the mirror, in the monocrystalline silicon layer, such that the hinges bridge the mirror and the frame; and forming a metal layer on at least a portion of the mirror and at least a portion of the frame, opposite the insulator layer. However, Minamoto teaches for example, a method of fabricating comprising: providing a silicon-on-insulator substrate that includes a monocrystalline silicon layer on a bulk silicon substrate, with an insulator layer (insulating film 110) therebetween; fabricating at least two spaced apart pads in the monocrystalline silicon layer that extend through the monocrystalline silicon layer to the insulator layer; fabricating at least one hinge (elastic member 152) on each of the at least two spaced apart pads; defining a mirror and a frame that at least partially surrounds the mirror, in the monocrystalline silicon layer, such that the hinges bridge the mirror and the frame; and forming a metal layer on at least a portion of the mirror and at least a portion of the frame, opposite the insulator layer (col. 7, ln. 1-20). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Krusius et al. with Minamoto to provide a method of fabricating a tiled array of MEM devices.

Re claim 13, supra claim 12. Minamoto further teaches for example, etching the bulk silicon substrate to expose the insulator layer adjacent the mirror and adjacent the pads (fig. 5A, col. 7, ln. 49-67, col. 8, ln. 1-11). It is a fundamental design choice to etch the insulator layer adjacent the mirror and the pads to release the mirror and the hinges.

Re claim 14, supra claim 13. Minamoto further teaches for example, the metal layer is a first metal layer, the method further comprising: forming a second metal layer on the mirror opposite the first metal layer (col. 7, ln. 49-67, col. 8, ln. 1-11). The office interprets the first metal layer to form the driving coil 104 (col. 7, ln. 13-16), which is opposite the mirror 106.

Re claim 15, supra claim 14. Krusius et al. further teach for example, mounting the silicon-on-insulator substrate on a base substrate (col. 6, ln. 38-67). It is a fundamental design choice to mount with the hinges and the first metal layer adjacent the base substrate and the second metal layer remote from the base substrate.

Re claim 17, Minamoto further teaches for example, a movable microeoectromechanical (MEM) structure comprising: etching an array of features in a silicon substrate; at least partially thermally oxidizing the array of features to form a pad comprising silicon dioxide (fig. 14B) in the silicon substrate; forming a movable MEM structure on the pad (col. 7, ln. 1-20); It is a fundamental step to release the movable MEM structure for use.

Re claim 18, supra claim 17. Minamoto further teaches for example, etching an array of features in a silicon layer on an insulator layer on a substrate (col. 7, ln. 1-20).

Re claim 19, supra claim 17. It is a fundamental design choice to make the features between about 5 μm and about 25 μm thick. Krusius et al. in view of Minamoto disclose the claimed invention except for making the features between about 5 μm and about 25 μm thick. It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the features between about 5 μm and about 25 μm thick, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Re claim 20, supra claim 18. Minamoto further teaches for example, a method wherein the removing comprises: etching the substrate adjacent the pad; etching the insulating layer adjacent the pad: and etching the pad from the insulating layer that was removed to the movable MEM structure (col. 7, ln. 1-20). The office interprets the teachings of Minamoto to include etching the substrate and etching the insulating layer and therefore teach the limitations set forth. Furthermore, it is a fundamental design choice to remove the MEM device by etching.

Claims 9-10 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krusius et al. in view of Minamoto in further view of Bhalla et al. in further view of Little.

Re claim 9, supra claim 8. But Krusius et al. in view of Minamoto in further view of Bhalla et al. fail to teach the mounting structure comprises a plurality of solder bumps that are configured to mount the plurality of MEM device substrates on the face. However Little teaches for example the mounting structure comprises a plurality of solder bumps that are configured to mount the plurality of MEM device substrates on the face (fig. 6A, col. 5, ln. 34-42). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Krusius et al., Minamoto, Bhalla et al. and Little in order to electrically and mechanically interconnect the devices.

Re claims 10 and 16, supra claim 9 and 15 respectively. Little further teaches for example, the MEM mirror substrates further comprises an underbump metallurgy between the frame and the solder bumps and wherein the underbump metallurgy and the metal layer on the MEM mirror substrate that is adjacent the base substrate both comprise a same metal and flip-chip mounting the silicon-on-insulator substrate on the base substrate using a plurality of solder bumps (fig. 6A, col. 5, ln. 34-42). The office interprets "flip-chip bonding process" as taught by

Little (col. 5, ln. 34-42) to teach solder bumps and underbump metallurgy to mechanically and electrically connect devices.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Martinez whose telephone number is 703-305-0577. The examiner can normally be reached on M-F 7:00 AM to 3:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Epps can be reached on 703-308-4883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7724 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-4883.

JPM
January 5, 2003

Hung Xuan Dang
Primary Examiner